In the Specification:

Please amend paragraph beginning on page 4, line 47 as follows:

In accordance with a first aspect, the present invention provides a memory device having a plurality of memory cells, wherein each memory cell has a trench capacitor formed in a semiconductor substrate and an access transistor ~~capacitor~~ for it, wherein each access transistor ~~capacitor~~ has a first contact region connected to an inner electrode of the trench capacitor, a second contact region connected to a bit line and a control electrode region, wherein the control electrode regions of neighboring access transistors are connected by a word line formed in the semiconductor substrate.

Please amend paragraph beginning on page 11, line 7 as follows:

As has been indicated above, the access transistor 18 preferably is a field effect transistor having a channel region 18e, wherein the control electrode region 18a of the access transistor 18, and thus the buried word line region 14d[[14c]], is separated from the channel region 18e of the access transistor 18 by the oxide layer 18b (gate oxide layer = GOX). The layer thickness of the oxide layer 18b is, for example, in a range of 0.5 to 15 nm and preferably in a range of 3 to 6 nm. An SiO_2 material is, for example, used as the material for the oxide layer, wherein any suitable isolation material having suitably selected layer thicknesses can be utilized depending on the respective selected setup of the access transistor.